SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR EXECUTING SHIFT REDUNDANCY OPERATION

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device having a shift redundancy function includes a switch circuit for changeably connecting a plurality of decode signal lines decoding an address signal to a plurality of selecting lines and redundancy selecting lines, and executes a switch operation for shifting at least one of a plurality of decode lines in the direction of a first redundancy selecting line positioned at one of the ends among a plurality of selecting lines or a second switch operation for shifting at least one of the decode lines in the direction of a second redundancy selecting line positioned at the other end among the selecting lines or both of the first and second operations when any fault occurs in a plurality of selecting lines. The semiconductor memory device preferably includes two or more first redundancy selecting lines positioned at one of the ends of a plurality of selecting lines, two or more second redundancy selecting lines positioned at the other end, and first and second switch units disposed in two stages. When any fault selecting line occurs, the first switch unit executes a first switch operation for shifting at least one of the decode signal lines in the direction of the first redundancy selecting line or a second switch operation for shifting the same in the direction of the second redundancy selecting line, or the second switch unit executes a third switch operation for shifting at least one decode signal line in the direction of the first redundancy selecting line or a fourth switch operation for shifting it in the direction of the second

redundancy selecting line.

2